

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: : Date: July 31, 2003
Marius K. Orlowski et al. : Attorney Docket No.: SC12885TP
Serial No.: : Art Unit:
Filing Date: : Examiner: Unassigned
For: METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE CHANNELS AND
STRUCTURE THEREOF

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

In accordance with 37 C.F.R. §1.56 and in compliance with 37 C.F.R. §§1.97 and 1.98, the references listed on attached Form PTO/SB/08 and/or subsequently identified herein, are being submitted herewith for consideration by the United States Patent and Trademark Office.

I. COPIES

- a. ☒ A legible copy of (i) each U.S. and foreign patents; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed, is included herewith.
- b. ☐ Any patents, publications or other information which are listed on PTO/SB/08 which are not enclosed herewith were previously cited by or submitted to the PTO in one of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. §120:

U.S. Serial Number

U.S. Filing Date

II. CONCISE EXPLANATION OF THE RELEVANCE (check at least one box)

- a. ☒ Except as may be indicated below in (b) of this section, all of the patents, publications or other information are in the English language (concise explanation not required).

- b. ☐ A concise explanation of the relevance of all patents, publications or other information listed that is not in the English language is as follows:
- c. ☐ The following additional information is provided for the Examiner's consideration:

III. ☐ CROSS REFERENCE TO RELATED APPLICATION(S)

The Examiner is advised that the following co-pending application(s) contain(s) subject matter that may be related to the present application. By bringing this (these) applications to the Examiner's attention, Applicant(s) does(do) not waive the confidentiality provisions of 35 U.S.C. §122.

Serial No.
10/074,732

Filing Date
02-13-2002

Art Unit
2815

FEES

IV. ☒ THIS IDS IS BEING FILED UNDER 37 C.F.R. §1.97(b): (check one box)

- a. ☒ within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) (37 C.F.R. §1.97(b)(1)). No fee or statement is required.
- b. ☐ within three months of the date of entry of the national stage as set forth in § 1.491 in an international application (37 C.F.R. §1.97(b)(2)). No fee or statement is required.
- c. ☐ before the mailing date of a first Office Action on the merits (37 C.F.R. §1.97(b)(3)). No fee or statement is required.
- d. ☐ before the mailing date of a first Office Action after the filing of a request for continued examination under § 1.114 (37 C.F.R. § 1.97(b)(4)). No fee or statement is required.

V. ☐ THIS IDS IS BEING FILED UNDER 37 C.F.R. §1.97(c): (check one box)

before the mailing date of either a Final Office Action under 37 C.F.R. §1.113 (See 37 C.F.R. §1.97(c)), or a Notice of Allowance under 37 C.F.R. §1.311 (See 37 C.F.R. §1.97(c)).

- a. ☐ No statement; therefore, charge deposit account 502117 the fee set forth in 37 C.F.R. §1.17(p).
- b. ☐ See the statement below. No fee is required.

VI. ☐ THIS IDS IS BEING FILED UNDER 37 C.F.R. §1.97(d):

on or before payment of the issue fee and is accompanied by the following:

- 1) a statement under 37 C.F.R. §1.97(e) as provided below;
- 2) Applicant(s) hereby a petition for consideration of this information disclosure statement; and
- 3) charge deposit account 502117 the petition fee set forth in §1.17(i).

VII. Statement under 37 C.F.R. §1.97(e) (check only one box, if applicable)
The undersigned hereby states that

- a. ☐ each item of information contained in the IDS was cited in a communication from a foreign Patent Office is a counterpart foreign application not more than three months prior to the filing of IDS; or
- b. ☐ no item of information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application, and to knowledge of the person signing the statement after making reasonable inquiry, no item of information contained in the IDS was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement, or
- c. ☐ some of the items of information contained in the IDS were cited in a communication from a foreign Patent Office. As to this information, the undersigned states that each item of information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this IDS. As to the remaining information, the undersigned hereby states that no item of this remaining information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application or, to the knowledge of the person signing the statement after making reasonable inquiry, no item of information contained in the IDS was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement.

VIII. PAYMENT OF FEES

- ☐ A check in the amount of _____ is enclosed for the above-identified fee(s).
- ☐ Please charge Deposit Account No. 502117 in the amount of \$180.00 for the above-indicated fee(s).
- ☒ If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 502117.
- ☐ Two Copies of this paper are attached for Deposit Account charges and debits.

The above references are being cited only in the interests of candor and without any admission that they constitute statutory prior art or contain matter which anticipates the invention or which would render the same obvious, either singly or in a combination, to a person of ordinary skill in the art.

If the Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule (with a petition if necessary) and charge the appropriate fee to Deposit Account No. 502117.

Respectfully submitted,
Marius K. Orlowski et al.


Robert L. King
Attorney for Applicant(s)
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Tel. (512) 996-3839

MOTOROLA, INC.
Customer Number 23125

Enclosures: ☒ PTO/SB/08
☒ 24 References AA-AX
☐ Foreign Search Report
☐ Other:

+

Please type a plus sign (+) inside this box. FORM PTO/SB/08

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				<i>Complete if Known</i>	
				Application Number	
				Filing Date	
				First Named Inventor	
				Group Art Unit	
				Examiner Name	
Sheet	1	of	3	Attorney Docket Number	SC12885TP

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

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Examiner Signature		Date Considered	
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation, if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.



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				Examiner Name	
Sheet	3	of	3	Attorney Docket Number	
				SC12885TP	

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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	AQ	JURCZAK, M. et al.; "Silicon-on-Nothing (SON) – an Innovative Process for Advanced CMOS"; IEEE Transactions on Electron Devices"; November, 2000; pp 2179-2187; Vol 47, No 11; IEEE	
	AR	FOSSUM, J.G. et al.; "Extraordinarily High Drive Currents in Asymmetrical Double-Gate MOSFETs"; Superlattices and Microstructures; 2000; pp 525-530; Vol 28; No 5/6; Academic Press	
	AS	JURCZAK, M. et al.; "SON (Silicon on Nothing) – A New Device Architecture for the ULSI Era"; Symposium of VLSI Technology Digest of Technical Papers; 1999; pp 29-30	
	AT	HUANG, X. et al.; "Sub 50-nm FinFET: PMOS"; IEDM; 1999; pp 3.4.1-3.4.4; IEEE	
	AU	HISAMOTO, D. et al.; "A Folded-Channel MOSFET for Deep-sub-tenth Micron Era"; IEDM; 1998; pp 1032-1034; IEDM	
	AV	TANAKA, T. et al.; "Ultrafast Operation of V_{th} -Adjusted $p^+ - n^+$ Double-Gate SOI MOSFET's"; IEEE Electron Device Letters; October 1994; pp 386-388; Vol 15, No 10; IEEE	
	AW	International Search Report	
	AX	Specification, abstract and drawings for Application No. 10/074,732 Filed February 13, 2002	

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				Marius K. Orłowski	
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Sheet	2	of	3	Attorney Docket Number	
				SC12885TP	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	AH	MONFRAY, S. et al.; "50nm-Gate All Around (GAA)-Silicon On Nothing (SON)-Devices: A Simple Way to Co-Integration of GAA Transistors Within Bulk MOSFET Process"; 2002 Symposium on VLSI Technology; 2002; pp 108-109; 2002 Symposium on VLSI Technology Digest of Technical Papers	
	AI	MONFRAY, S. et al.; "Highly-Performant 38nm SON (Silicon-On-Nothing) P-MOSFETs with 9nm-thick Channels"; 2002 IEEE International SOI Conference; 10/02; pp 20-22	
	AJ	MONFRAY, S. et al.; "SON (Silicon-On-Nothing) P-MOSFETs with Totally Silicided (CoSi ₂) Polysilicon on 5nm-thick Si Films: The Simplest Way to Integration of Metal Gates on Thin FD Channels"; IEDM; 2002; pp 263-266; IEEE	
	AK	YU, Bin et al.; "FinFET Scaling to 10nm Gate Length"; IEDM; 2002; pp 251-254; IEEE	
	AL	KEDZIERSKI, Jakub et al.; "High_Performance Symmetric-Gate and CMOS-Compatible V _t Asymmetric-Gate FinFET Devices"; IEEE; 2001; 4 pp	
	AM	CHOI, Y. et al.; "Sub-20nm CMOS FinFET Technologies"; IEDM; 2001; pp 19.1.1-19.1.4; IEEE	
	AN	KIM, K. et al.; "Double-Gate CMOS: Symmetrical-Versus Asymmetrical-Gate Devices"; IEEE Transactions on Electron Devices; February, 2001; pp 294-299; Vol 48, No 2; IEEE	
	AO	MONFRAY, S. et al.; "First 80nm SON (Silicon-On-Nothing) MOSFETs With Perfect Morphology and High Electrical Performance"; IEDM; 2001; pp 29.7.1-29.7.4; IEEE	
	AP	HISAMOTO, D. et al.; "FinFET-A Self-Aligned Double-Gate (MOSFET) Scalable to 20nm"; IEEE Transactions of Electron Devices; December 2000; pp 2320-2325; Vol 47, No 12; IEEE	

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